High Performance BGP Security: Algorithms and Architectures

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NANOG-69, February 2017, Washington DC

Antara Teknik LLC contribution to this work was supported by the National Institute of Standards and Technology (NIST) under an SBIR cooperative agreement 70NANB14H289. NIST’s research was supported by the Department of Homeland Security under the Secure Protocols for the Routing Infrastructure (SPRI) program and the NIST Information Technology Laboratory Internet Infrastructure Protection Program.
BGP Vulnerabilities

Border Gateway Protocol is vulnerable to malicious attacks that target the control plane

- Prefix/sub-prefix hijacks
  - Steers traffic away from legitimate servers
- Prefix squatting
  - Hijacks a not-in-service prefix and sets up spam servers
- AS path modification (Man-in-the Middle) attacks
  - Modifies AS path causing data to flow via the attacker
- Route leaks
  - Announces routes in violation of ISP policy, thereby redirecting traffic via the attacker

The exploitations commonly result in DoS, spam, misrouting of data traffic, eavesdropping on user data, etc.
Objectives of the IETF SIDR WG Security Solution

• Verify that the originating AS shown in the announcement is authorized to originate the prefix [RFC 6811]
• Verify that the BGP announcement did indeed traverse a sequence of ASs as shown by AS path in the announcement -- BGPsec [1]
• Provide protection from withdrawal suppression and malicious replay attacks [4]
• Accommodate special cases such as:
  – Transparent Route Servers (RS) at Internet Exchange Points (IXP)
  – An AS confederation must be visible externally as a single public AS
• Provide route-leak detection capability (as best as possible) [5]

Key Elements of the Security Solution

- Hierarchical certificate chain for resource allocations
  - IP address blocks (prefixes)
  - Autonomous system numbers
- Resource PKI (RPKI) repository
- Prefix owner signs a Route Origin Authorization (ROA) authorizing an AS to originate one or more prefixes
  - ROA: {ASN; Prefix1, maxLength1; Prefix2, maxLength2}
- Each BGPsec speaker uses its private key to sign updates it is propagating to its peer AS
- Receiving router validates the origin using ROA information
- Receiving router also performs path validation by verifying the AS path signatures in updates

RPKI provides provenance and integrity.
AS Path Protection: Basic Principle of BGPsec AS Path Signing

Route Origin Authorization (ROA): (10.1.0.0/16, AS1, maxlength=18)
ROA is a signed object; stored in RPKI repository
* Next hop AS (Target AS) signed over but not carried in the

Note: For the precise BGPsec update format and details, see BGPsec specification
BGPsec_Path Attribute Format

- Secure_Path Length
- pCount-n
- Flags-n
- ASN-n
- ...
- pCount-1
- Flags-1
- ASN-1

Signature_Block Length
ALGORITHM SUITE ID
SKI-n
Signature-n Length
Signature-n
- ...

SKI-1
Signature-1 Length
Signature-1

- pCount is AS prepend count; pCount = 0 for transparent route server
- Flags: Confed_Flag set to indicate inter-AS hop within an AS confederation
BGPsec Compute Resource Estimation

• BGP router receives approx. 680K prefixes [9] from each of its transit ISPs with an average path length of approx. 4 hops [8]

• Internet contains about 55K ASs [8]

• A typical BGPsec router:
  – Verifies on average four signatures per supported algorithm, per update (two supported algorithms are allowed)
  – Generates one new signature per supported algorithm, per update
BGPsec Compute Resource Estimation (cont.)

• For Update Signing: Each AS will need at least one signing (private) key per supported algorithm...
  – Worst case: private key per router
  – Must be maintained securely (per NIST SP800-130, Confidentiality and Integrity)

• For Update Validation: an average of four public keys per supported algorithm need to be loaded
  – Public key retrieval includes public key database access and ECC Public-Key Validation (per NIST SP800-56A) per key
  – Caching helps
BGPsec Path Sign Ops

Path

Algorithm 1
Sign Operation

Algorithm 1
Signature \((r,s)\)

ASN1 Encode Operation

One Time Secret Number

Private Key

Domain Parameters

Algorithm 2
Sign Operation

Algorithm 2
Signature \((r,s)\)

ASN1 Encode Operation

Algorithm 1 Signature

Algorithm 2 Signature

One Time Secret Number

Private Key

Domain Parameters
Optimizations

• Multi-level Optimizations are required to maximize performance
  – System Level Optimizations
    • Asynchronous operations across cores
    • Parallel multi-segment path verifications
    • High Integrity Public key management system
  – Algorithmic Optimizations
    • Early termination on Invalid segment (BGPsec Algorithm)
    • Pre-calculations for ECDSA sign Operation (ECDSA Algorithm)
  – Group Level Optimization
    • Ultra fast, secure Point Multiplication (e.g., Side Channel Attack (SCA) Resistant Fixed-base_NAF Windowing Method for Point Multiplication)
  – Field Level Optimizations
    • Special forms of domain parameters (e.g., Generalized Mersenne Primes)
    • Barrett Reduction modulo p and/or Montgomery w-by-w modulo

Optimizations must maintain and enhance the security of the implementation under all use-cases
Example Algorithmic Optimization

Observation:
The most compute intensive ECDSA sign calculations do not have any dependency on the “message” to be signed.

Options:
1. Pre-compute $r$ and “safely” store
2. Asynchronously compute $r$ on a different core
3. Proprietary methods

Considerations:
- Secure implementations are not trivial

Substantially reduces sign op latency
Example Group Level Optimizations

Pre-Calculation:
Take \((K_{d-1}, \ldots, K_1, K_0)_{2}^w\) as the base \(2^w\) representation of \(k\),
where \(d = \lceil (m/w) \rceil\), then
\[kP = \sum_{i=0}^{d-1} K_i(2^{wi} P)\]
For each \(i\) from 0 to \(d-1\),
pre-calculate \(j\) number of points,
where
\[j = \frac{2^{w+1} - 2}{3}\] if \(w\) is even;
\[j = \frac{2^{w+1} - 1}{3}\] if \(w\) is odd

Evaluation:
INPUT: NAF\((k)\), \(d\), \(pT\) (Pointer to pre-computed data table)
OUTPUT: \(A = kP\).
1. Evaluation: \(A \leftarrow O\)
2. For \(i\) from 0 to \(d-1\) do
   2.1 SafeSelect \((Pi)\),
      use \(K_i=j\) to choose the appropriate \(P[i][j]\) from \(Ptable\) (handle \(-j\))
   2.2 \(A \leftarrow A + Pi\)
3. Return\((A)\)

Traditional Right to Left Binary Method for Point Multiplication
   Evaluation time: \((0.5m)pA + (m)pD\)
P-256 Eval. time: \(128pA + 256pD\)
Not SCA resistant

Fixed-base NAF Windowing Method for Point Multiplication
   Evaluation time: \((0.5m)pA + (m)pD\)
P-256 Eval. time: \(~64pA\)
SCA resistant

\(m\): number of bits; \(pA\): multi-precision point addition; \(pD\): multi-precision point double
**taraEcCRYPT™ Performance**

- One of the fastest available libraries for ECDSA P-256 and P-384 operations
- Thread-safe dynamic library
- Single core performance numbers are captured with a standalone utility to show the best possible rates

<table>
<thead>
<tr>
<th>ECDSA Ops</th>
<th><em>tara</em> EcCRYPT-3 P-256 Rate (ops/sec)</th>
<th><em>tara</em> EcCRYPT-3 P-384 Rate (ops/sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sign Operation with provided Hash</td>
<td>46,191.83</td>
<td>19,433.85</td>
</tr>
<tr>
<td>Sign Op including Hash gen Op</td>
<td>40,076.27</td>
<td>18,163.09</td>
</tr>
<tr>
<td>Sign Op including Hash gen Op, but using pre-calculated random-number</td>
<td>48,257.51</td>
<td>21,287.04</td>
</tr>
<tr>
<td>Verify Op with provided Hash</td>
<td>32,895.25</td>
<td>10,954.57</td>
</tr>
<tr>
<td>Verify Op including Hash gen Op</td>
<td>29,521.49</td>
<td>10,706.65</td>
</tr>
</tbody>
</table>

System used for all test results:
- Intel® Xeon® CPU E3-1285 v4 at 3.5GHz; 16GB Memory; Centos 7; gcc 5.2
- Test results on single core; Hyper-threading and Turbo features turned off; Nominal message size 1024 bytes
openSSL vs. taraEcCRYPT™ Performance

(With provided hash in all cases)

System used for all test results:
- Intel® Xeon® CPU E3-1285 v4 at 3.5GHz; 16GB Memory; Centos 7; gcc 5.2
- Test results on single core; Hyper-threading and Turbo features turned off
• Measured operation includes:
  - Assembly of the BGPsec Path data to be signed
  - Hash of path data
  - Execution of Path_Signature operation using ECDSA P-256 or P-384
  - ASN1 encode of signature(s)

• On a single core using taraEcCRYPT Sign with pre-calculated random-number:
  - P256 Path sign performance is over 40k signatures/sec
  - P384 Path sign performance is over 20k signatures/sec

• Given current performance levels, multi-core parallelization may not be needed to sustain a high number of signature operations.
  - However, proper random numbers can be pre-calculated asynchronously on any available core

Same system utilized to generate the test results as on slide #15.
**taraBGPsec™ Path Verify Performance**

Measured operation includes:

- BGPsec related parsing of update packets
- Fetching public keys with assured integrity
- Execution of Path_Segment_Verify operations (*taraVerifyParallel*)
  - Early termination if any Segment of the path is found to be Invalid
  - Two signature algorithms (P-256 and P-384) can be supported

---

**Signature Segment Verify Speed (OPS/S)**

<table>
<thead>
<tr>
<th># CORES</th>
<th>SPEED (OPS/S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>24649</td>
</tr>
<tr>
<td>2</td>
<td>48039</td>
</tr>
<tr>
<td>3</td>
<td>59712</td>
</tr>
<tr>
<td>4</td>
<td>77972</td>
</tr>
</tbody>
</table>

Same system utilized to generate the test results as on slide #15, except the number of cores is varied.
BGPsec Contribution to Convergence Time

BGPsec update processing is **Additive** to Traditional BGP processing

We focus here on the incremental CPU cost due to BGPsec
BGPsec Verify / Sign Speed (Updates/s)

- taraBGPsec
- Xeon® CPU E3-1285 v4 3.5GHz (using only one core)
Validation Cost Model

- taraBGPsec
- Xeon® CPU E3-1285 v4 3.5GHz (using only one core)

<table>
<thead>
<tr>
<th>AS path length</th>
<th># Prefixes announced</th>
<th>Processing time (sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1353</td>
<td>0.0549</td>
</tr>
<tr>
<td>2</td>
<td>21586</td>
<td>1.7515</td>
</tr>
<tr>
<td>3</td>
<td>6820</td>
<td>0.8301</td>
</tr>
<tr>
<td>4</td>
<td>1627</td>
<td>0.2640</td>
</tr>
<tr>
<td>5</td>
<td>942</td>
<td>0.1911</td>
</tr>
<tr>
<td>6</td>
<td>45</td>
<td>0.0110</td>
</tr>
<tr>
<td>7</td>
<td>14</td>
<td>0.0040</td>
</tr>
<tr>
<td>8</td>
<td>6</td>
<td>0.0019</td>
</tr>
</tbody>
</table>

Total (seconds) = 3.11

CPU Time on R if Session to A is Reset

<table>
<thead>
<tr>
<th>AS path length</th>
<th># Prefixes announced</th>
<th>Processing time (sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>620</td>
<td>0.0252</td>
</tr>
<tr>
<td>2</td>
<td>16028</td>
<td>1.3005</td>
</tr>
<tr>
<td>3</td>
<td>9434</td>
<td>1.1482</td>
</tr>
<tr>
<td>4</td>
<td>2922</td>
<td>0.4742</td>
</tr>
<tr>
<td>5</td>
<td>435</td>
<td>0.0882</td>
</tr>
<tr>
<td>6</td>
<td>46</td>
<td>0.0112</td>
</tr>
<tr>
<td>7</td>
<td>15</td>
<td>0.0043</td>
</tr>
<tr>
<td>8</td>
<td>27</td>
<td>0.0088</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>0.0004</td>
</tr>
</tbody>
</table>

Total (seconds) = 3.06

CPU Time on R if Session to C is Reset
Need not Sign To Stubs

Only needs to have appropriate ROAs registered and own Private Key;
No other crypto or RPKI data
No Hardware Upgrade!!
What Fraction are Stub ASs?

For all years, 84% of all ASs were Stubs
CPU Cost for Validation and Signing

- **ISP A and A’s Customer Cone (Large Global ISP)**

<table>
<thead>
<tr>
<th>AS path length</th>
<th># Prefixes announced</th>
<th>Processing time (sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1353</td>
<td>0.16</td>
</tr>
<tr>
<td>2</td>
<td>21586</td>
<td>3.37</td>
</tr>
<tr>
<td>3</td>
<td>6820</td>
<td>1.34</td>
</tr>
<tr>
<td>4</td>
<td>1627</td>
<td>0.39</td>
</tr>
<tr>
<td>5</td>
<td>942</td>
<td>0.26</td>
</tr>
<tr>
<td>6</td>
<td>45</td>
<td>0.01</td>
</tr>
<tr>
<td>7</td>
<td>14</td>
<td>0.01</td>
</tr>
<tr>
<td>8</td>
<td>6</td>
<td>0.00</td>
</tr>
<tr>
<td><strong>Total (seconds)</strong></td>
<td></td>
<td><strong>5.54</strong></td>
</tr>
</tbody>
</table>

CPU workload on R, including Validation & Signing, if session to A is reset.

- R peers with 3 non-stub BGPsec peers
- R’s other peers are stub ASs

**Hardware specs:**
- taraBGPsec
- Xeon® CPU E3-1285 v4
- 3.5GHz (using only one core)
Conclusions

• Industry leading high performance BGPsec implementation architected and algorithmically optimized

• Other factors expected to contribute to efficient BGP/BGPsec convergence in future:
  ❑ Multi-threading and use of multiple cores in route processors
  ❑ Update processing optimizations, e.g. caching results of verification
  ❑ Enhanced Graceful Restart [10]
Thank you.

Questions?
References

   Workshop on ECC Standards,
5. K. Sriram, D. Montgomery, B. Dickson, K. Patel, and A. Robachevsky, "Methods for Detection and
6. K. Sriram and Randy Bush, "Estimating CPU Cost of BGPSEC on a Router," presented at the RIPE 63,
   at the IETF-91 Joint IDR/SIDR WG Meeting, November 2014.
11. A. Lambrianidis and E. Nguyenduy, “Route server implementations performance,” 20th Euro-IX Forum,
    Amsterdam, NL, April 2012.
Backup Slides
Example Field Level Optimizations

- Multi-precision regular/constant time add and subtract modulo prime ops are best implemented in x86-assembly
  - Any Carry or Borrow is easily detected
  - Handled by instructions such as “adcq” and “sbbq”
- Optimized multi-precision multiply and square operations are a must for high performance

Traditional 64-bit multiply in x86

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>mov OP, [pB+8*0]</td>
<td>add R0, rax</td>
</tr>
<tr>
<td>mov rax, [pA+8*0]</td>
<td>add rdx, 0</td>
</tr>
<tr>
<td>mul OP</td>
<td>mov TMP, rdx</td>
</tr>
<tr>
<td>add R0, rax</td>
<td>mov pDst, R0</td>
</tr>
<tr>
<td>adc rdx, 0</td>
<td>mov rax, [pA+8*1]</td>
</tr>
<tr>
<td>mov rdx, rdx</td>
<td>mul OP</td>
</tr>
<tr>
<td>mov pDest, rdx</td>
<td>mov rdx, [pB+8*0]</td>
</tr>
<tr>
<td>mov rax, [pA+8*1]</td>
<td>mul OP</td>
</tr>
<tr>
<td>mul OP</td>
<td>add R2, rax</td>
</tr>
<tr>
<td>add R0, rdx</td>
<td>adc TMP, 0</td>
</tr>
<tr>
<td>add R1, rax</td>
<td>add R2, R0</td>
</tr>
<tr>
<td>adc R0, 0</td>
<td>adc TMP, 0</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>

64-bit multiply with Broadwell Inst.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>xor rax, rax</td>
<td>mulx T1, R1, [pA+8*2]</td>
</tr>
<tr>
<td>mov rdx, [pB+8*0]</td>
<td>addox R1, R2</td>
</tr>
<tr>
<td>adc R0, 0</td>
<td>adcx R3, T1</td>
</tr>
<tr>
<td>mov rdx, [pB+8*0]</td>
<td>mulx T1, T2, [pA+8*0]</td>
</tr>
<tr>
<td>mov rdx, [pB+8*0]</td>
<td>addox R0, T2</td>
</tr>
<tr>
<td>adc R1, T1</td>
<td>adcx R1, T1</td>
</tr>
<tr>
<td>mov pDest, R0</td>
<td>mov pDest, R0</td>
</tr>
<tr>
<td>...</td>
<td>mulx T1, R0, [pA+8*1]</td>
</tr>
<tr>
<td>addox R0, R1</td>
<td>adcx R2, T1</td>
</tr>
</tbody>
</table>