The Open Source LSR

Scott Whyte
swhyte@google.com
What is an "Open Source LSR"?

- MPLS Label Switching Router
- Running OSPF, LDP
- Hardware Forwarding (4 x 1GigE ports)
- Open Source Software AND Hardware
Why build one?

- Most of the parts already exist
- Create community involvement
- Enable interesting network research
- Hardware usually the stopper
Components

- NetFPGA
- OpenFlow
- mpls-linux
- quagga-ldp
- LSP Synchronizer
Components: NetFPGA

- ZBT SRAM (4.5MB)
- Virtex-II Pro FPGA
- SATA
- 4x 1GigE links
- BCM 5464
- PCI
- DDR2 SDRAM (64MB)
Components: MPLS OpenFlow

Programming the flow table with OpenFlow:

```
OpenFlow Controller

OpenFlow kernel module

NetFPGA Driver

OpenFlow Switch

Hardware
```
Components: MPLS OpenFlow

Programming the flow table with OpenFlow:

Kernel LFIB  OpenFlow Controller

OpenFlow kernel module

NetFPGA Driver

OpenFlow Switch

Hardware
Components: MPLS OpenFlow and NetFPGA

- match = match on some MPLS label
- action = rewrite label and forward
Components: MPLS OpenFlow and NetFPGA

Packets for host sent to kernel

OSPF, LDP, ssh, etc.
Components: mpls-linux

- Patches for kernel (2.6.32.16)
- Source for building MPLS kernel modules
- Patches for iproute2
  - Updated 'ip' command
  - New 'mpls' command
Components: quagga-ldp

- Standard quagga provides OSPF
- This project adds LDP support

- LDP Parameters used:
  - Downstream unsolicited
  - Liberal retention
  - Ordered control
Components: LSP Synchronizer

- **quagga provides:**
  - labels via ldpd
  - kernel LFIB updates via zebrad

- **OpenFlow provides:**
  - FIB programming on NetFPGA

- **LSP Synchronizer has to:**
  - Scan kernel LFIB
  - Compare to FIB on NetFPGA
  - Update FIB as needed
Open Source LSR

User Space:
- LSP Synchronizer
  - dpctl
  - mpls
- OSPF
- LDP
- Zebra
- RIB

Kernel Space:
- NetFPGA OpenFlow module
- NetFPGA Driver

Hardware Land:
- Port 0
- Port 1
- Port 2
- Port 3
- PCI
- NetFPGA-1G Board
- OpenFlow MPLS Switch bitfile on FPGA
Open Source LSR
Open Source LSR

User Space
- LSP Synchronizer
  - dpctl
  - mpls
- OSPF
- LDP
- Zebra
  - RIB

Kernel Space
- NetFPGA OpenFlow module
- NetFPGA Driver
- MPLS modules
  - entry 0
  - entry 1
  - entry n
  - Label FIB

Hardware Land
- Port 0
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Software vs. Hardware Forwarding

- Simple Test
- Bidirectional Throughput
- 68 byte packets
- 1504 byte packets
Software vs. Hardware Throughput

1504 Byte Packets

- **Software RX bps** (blue line)
- **Hardware RX bps** (red line)
Software vs. Hardware Throughput

68 Byte Packets

- Software RX bps
- Hardware RX bps
Lab Topology: Verifying MPLS

- OSPF on all devices
- LDP on all devices
- Juniper M10
- Redback SmartEdge100
Lab Topology: BGP-free core

- OSPF on all devices
- LDP on all devices
- Juniper M10s as LERs
- iBGP across LSRs
LER?

Hardware allows popping and pushing too...
Future Work

● Near-term
  o Bugfixes
  o 64-bit Linux kernel
  o Port to BSD
  o RSVP-TE support in Quagga
  o 10G NetFPGA card

● Medium-term
  o Centralized control plane via an OpenFlow controller
  o BGP-free core design based on open-source LSRs
Download!

- This project tarball
  - http://code.google.com/p/opensource-lsr/

- Open-source projects integrated in this project
  - mpls-linux
    - http://repo.or.cz/w/mpls-linux.git
  - quagga-ldp
    - http://repo.or.cz/w/jleu-quagga.git
  - NetFPGA / OpenFlow with MPLS support
    - http://netfpga.org/foswiki/bin/view/NetFPGA/OneGig/ProjectsOpenFlowMPLSSwitch
Credits

● The Open Source Projects
  o mpls-linux
  o quagga-ldp
  o OpenFlow-MPLS
  o NetFPGA

● LSP synchronizer, debugging - Jonathan Ellithorpe

● Lab Testing - Richard Hay

● Overall Concept - Stephen Stuart