Panel: 100Gbps Forwarding Architecture Challenges

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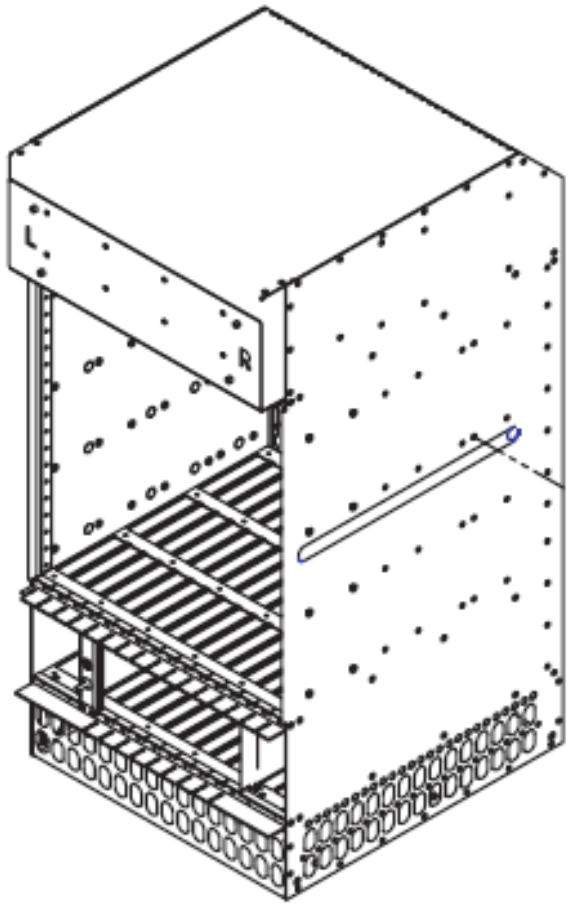
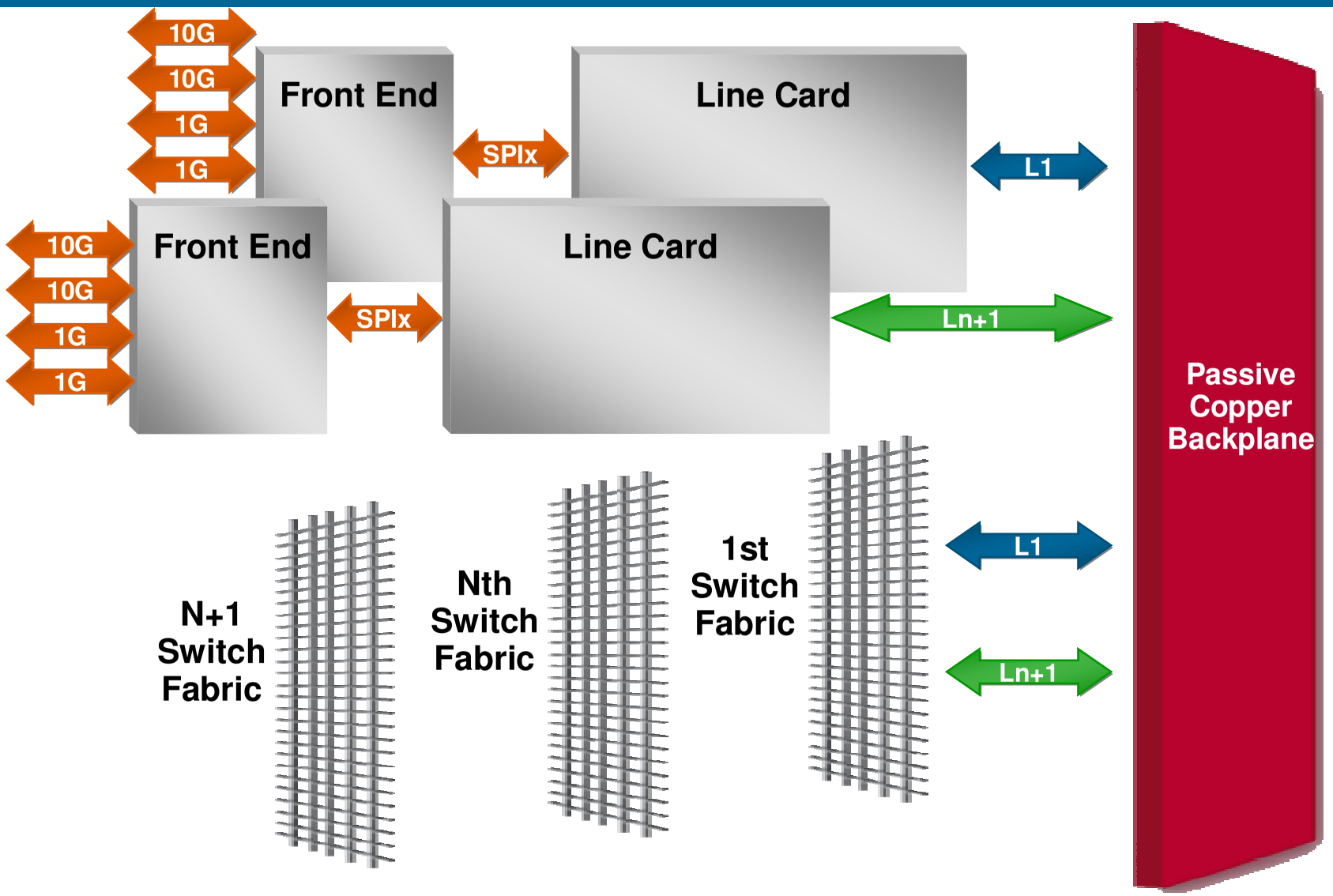
Anatomy of a 100 Gbps Solution: Chassis Design

- Chassis design issues to consider
  - Backplane and channel signaling for higher internal speeds
  - Lower system BER
  - Connectors
  - N+1 switch fabric
  - Reduced EMI
  - Clean power routing architecture
  - Thermal and cooling
  - Cable management
- All design aspects must also meet local regulatory standards



System Implementation: N+1 Fabric Architecture



Anatomy of a 100 Gbps Solution: ASIC Selection

- High speed ASIC interfaces
  - Interfaces between ASICs, backplane, and memory will use SERDES
  - Higher speed SERDES needed to reduce pin and gate count between chips
  - 400 to 500 Gb/s per slot will exasperate the need for narrower interfaces,i.e. higher speed signaling!