Panel: 100G Forwarding Architecture Challenges With QoS, Policer Examples

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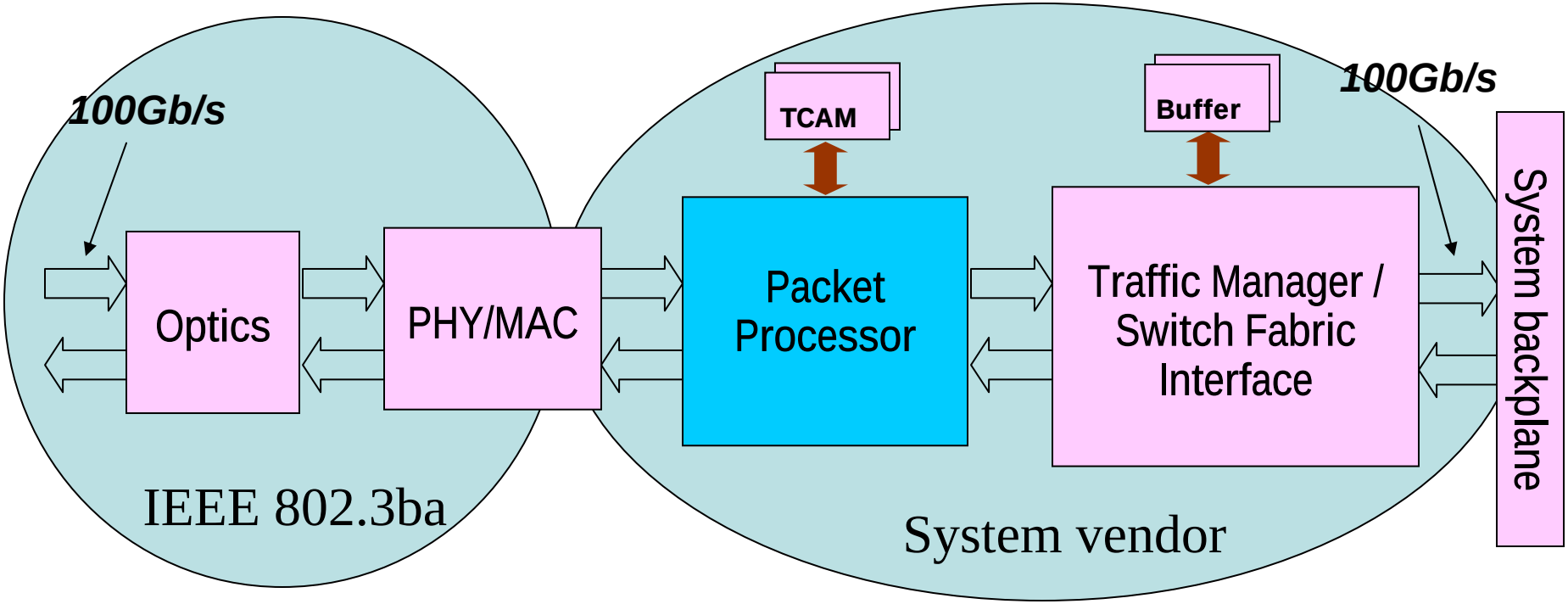
Agenda

- Key Components
- Challenges
- Potential Solutions

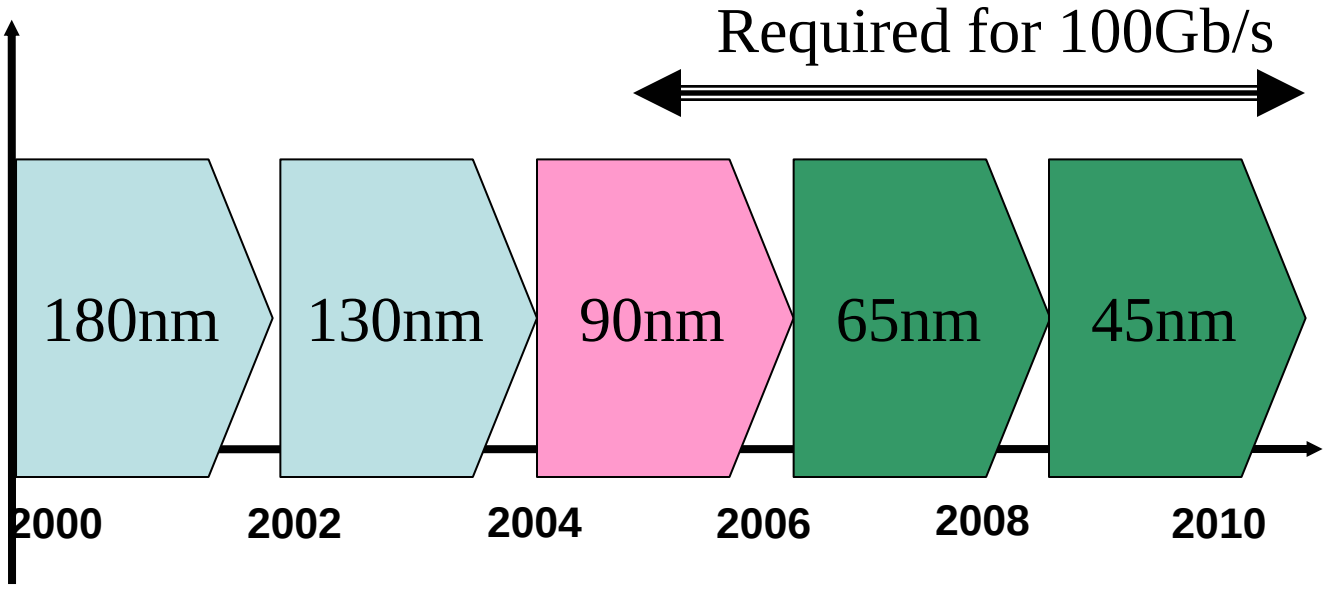
Key components required for 100G

- Optics, PHY/MAC
- Packet Processor
- Traffic Manager / Switch Fabric Interface
- System Backplane

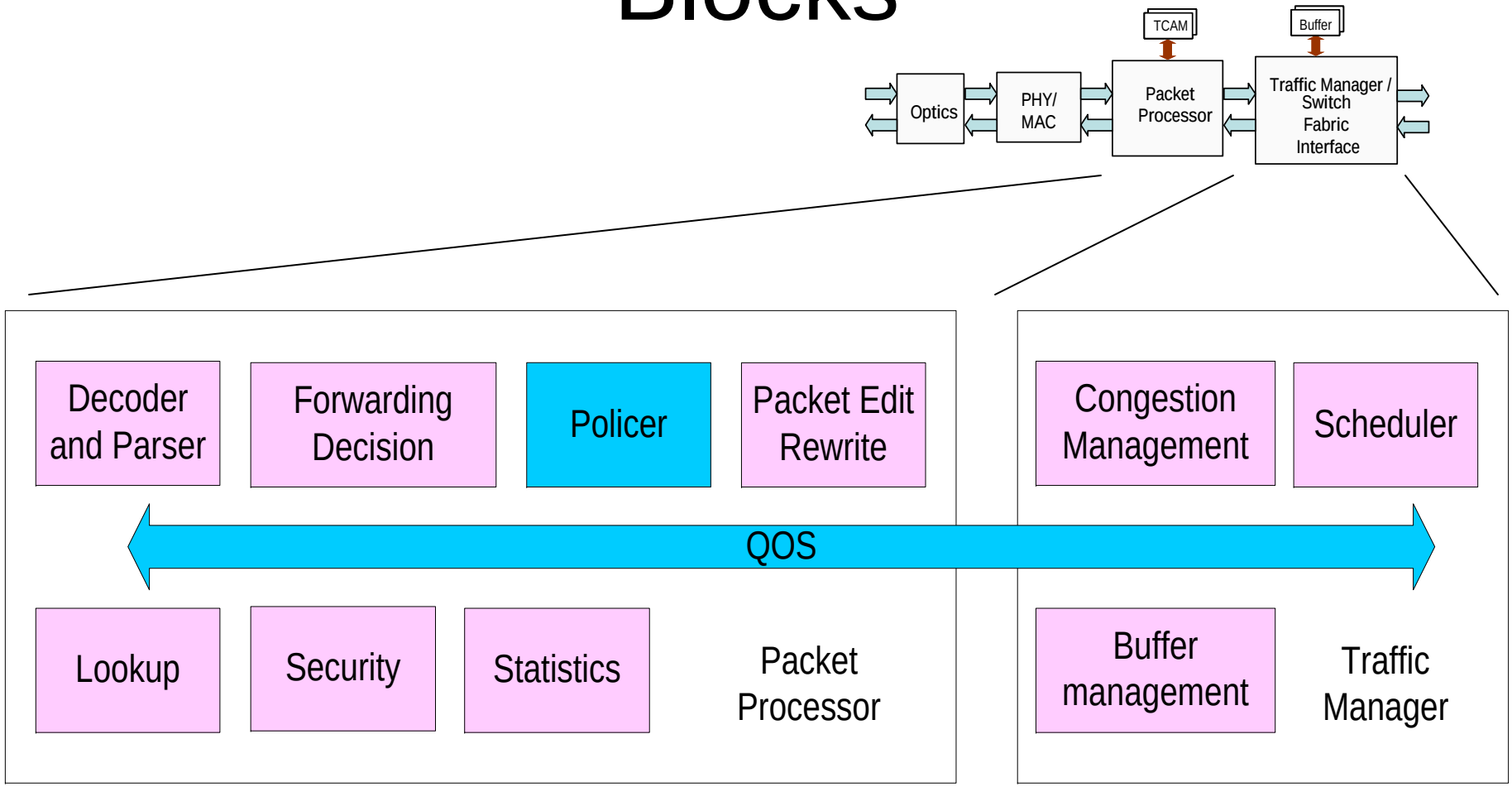


CMOS ASIC Process Technology

- Supporting chips (Phy/MAC, Packet Processor, Traffic Manager) will need to run at higher speeds to support 100Gb/s data rates
- 65nm - 45nm technology enables higher speed chip to chip signaling allowing for greater bandwidth and lower power



100GE Processing – Building Blocks



100GE Processing – Building Blocks

- Building Blocks
  - Packet Decoders and Parsers, Lookup Engine
  - Forwarding Decision, Bridging, Routing,…
  - Policer, QoS
  - Packet Editing and Rewriting
  - Buffer manager, congestion management, scheduling
- Policer and QoS are some of many challenges at 100G

QoS at 100G

- QoS to manage flow and provide differentiated services, it is important at 100G
- QoS are typically distributed among packet processing and traffic manager
- E.g. Decoder/Parsers extract .1p, DSCP and/or Label CoS, priority mapping etc.
- Packet processor conveys priority and drop precedence info to traffic manager

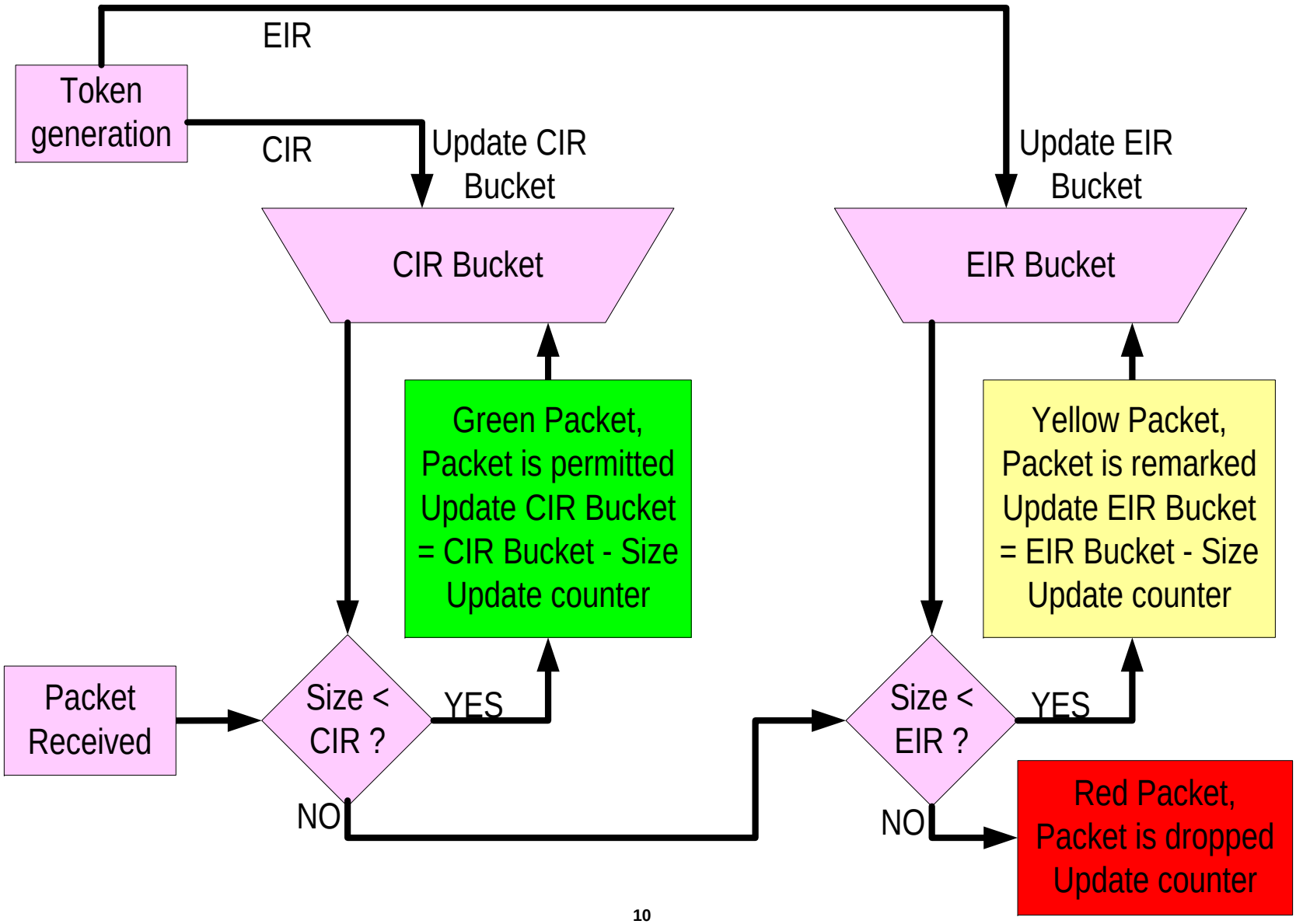
QoS considerations at 100G

- Prioritization
  - Priority and drop precedence must be determined at 100G
- Traffic Policer
  - More details in next few slides
- Congestion management
  - WRED, Tail-drop, etc must work at 100G
- Scheduling
  - Shaper and Scheduler with WRR, SP and hybrid WRR need to be able to handle traffic at 100G

100G Policer – Review at 10G

- Typically dual leaky bucket algorithm
- Decisions
  - Forward, Drop packet
  - Mark Green, Re-mark Yellow or Red
- Accounting
- 10GE maximum packet rate 15Mpps
- Typically require multiple memory read and write operations per packet
- Fairly straightforward to implement at 10G

100G Policer – Illustration



The Challenges at 100G

- 100GE Packet rate up to 150Mpps
- In design perspective, dual leaky bucket algorithm can be compute intensive and timing critical to implement at this rate
- Similarly, there are challenges to prioritization of packets, congestion management and scheduling, and the rest of building blocks.

Potential Solutions

- Technology node at 65nm or below reduce power consumption and ease timing challenge
- Divide-and-conquer, multiple instantiations of policer, need to load balance and keep coherent bucket contents
- Pipelining implementations, dividing processing task and reduce cycle time. Resulting in higher throughput

Summary

- Customers need 100G interface to keep up with network growth
- High-level block diagram
- Challenges in forwarding architecture
  - Process Higher Packet Rate and Bandwidth
- Potential Solutions – Combination of process technology and design innovation

Thank you!